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CDMS Analog Feedback FPGA Register Map

0. Trigger threshold register

The value in this register is the signal threshold (in ADC counts) at which a self trigger will occur. The phonon threshold is a signed number with a span of -128 to +127, to accommodate the polarity setting of the feedback loop. The charge threshold is an unsigned number with a span of 0 to 255.

15:8	7:0
Charge Threshold	Phonon Threshold

1. Device Data

A write puts data into a register for serial transmission to the CPLD resident on the analog portion of the board. It also begins the transmission of the data and the device number.

2. Device Address

Bits 3:0 represent the device number of various DACs and switches on the analog portion of the board (See Wayne Johnson's CPLD map for details).

3. Input FIFO CSR Register

Bits 3:0 Empty flags for the four phonon input fifos Bits 3:0 correspond to channels D:A
Bits 7:4 Full flags for the four phonon input fifos Bits 3:0 correspond to channels D:A
Bits 9:8 Empty flags for the four charge input fifo Bits 9:8 correspond to channels O:I
Bits 11:10 Empty flags for the four charge input fifos Bits 11:10 correspond to channels O:I
Bit 12: Arm data taking until internal test pulse cycle boundary, or external trigger arrives
Bit 13: Send a sync pulse to the ADCs
Bit 14: Reset Input fifo state machine, start writing of data to the SDRAM
Bit 15: Software trigger. SDRAM writes stop after specified number of post store samples

15	14	13	12	11:10	9:8	7:4	3:0
Software trigger	Fifo Reset	ADC sync	Arm data taking. Start on external trig, triangle start	Charge data fifo Full flags	Charge fifo Empty flags	Phonon fifo Full flags	Phonon fifo empty flags

4. Test Pulse Magnitude Register

Test pulse magnitude register. This is a 15 bit read/write register. The full scale is approximately 200mV at the input of the feedback amplifier.

5. Test Pulse Ramp Rate Register

This 8 bit register sets the slope (1/frequency) of the test pulse triangular waveform.

6. LED flasher pulse Width Register

This 10 bit register sets the width of the LED flasher pulse in units of 10us.

7. LED flasher repetition rate register

This 16 bit register sets the repetition rate of the LED flasher in units of 20us.

8. Trigger address high

Bits 20..16 the pointer to the SDRAM data within a channel sector at the time a trigger occurred.

9. Trigger address low

Bits 15..0 of the SDRAM write address at the time a trigger occurred.

A. SDRam Data Register

Read of 16 bit SDRam data

B. SDRAM Address 23:16

The ADC data is written into six separate channel pages: 0 – Phonon A, 0x20 – Phonon B, 0X40 – Phonon C, 0x60 – Phonon D, 0x80 – Charge I, 0xC0 – Charge O

C. SDRAM Address 15:0

A to write this location completes the 24 bit address definition and starts a transfer of ADC data to an output FIFO starting at the specified address. With the transfer of each word, the SDRAM address increments, modulo the channel page. A read from this location will show the address most recently used to write SDRAM data into the output FIFO.

D. General purpose CSR register

Bits 2:0 set the data direction (transmit or receive) of the 3 bit LVDS bus. A “0” sets the direction to receive, a “1” to transmit.

Bits 4:3 determine which reference is used to lock the VXO frequency. 00: no external reference, the VXO tuning voltage is set to the middle of its range. 01: the reference in the external frequency LEMO connector. 10: the reference is bit 0 of the LVDS bus. 11: not defined.

Bit 5: This bit enables the triangle wave generator.

Bits 7:6 Enable the LED flasher for LED1 and 2 1=enabled, 0=disabled

Bit 8 : Run flasher once (bit=1) or repeat indefinitely (bit=0)

Bit9: Change data taking from normal (bit=0) to averaging ADC samples by 128 (bit = 1).

15:12	9	8	7	6	5	4:3	2:0
Not Used	Enable Average by 128	Single Step/Free Run	LED 2 Pulser Enable	LED 1 Pulser Enable	Test Pulse Enable	PLL Reference Source	LVDS bus direction control

E. ADC record length

This is a 16 bit counter that counts 8 phonon ADC words and 16 charge ADC words per count. The power up default value is 0x1FF which corresponds to 4096 phonon words and 8192 charge words.

F. Baseline length, trigger contributors

Bits 13:7 Select which channels contribute to a trigger. A 0 to all bits disables the self trigger

Bits 6:0 The number of samples to average in order to establish a baseline the range is 1..63

15:14	13	12	11	10	9	8	7	6:0
Not Used	QO	QI	Ph D	Ph C	Ph B	Ph A	Not Used	# of samples used to establish a baseline